REMARKS

Claims 1-22 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the remarks contained herein.

Applicant would like to thank the Examiner for courtesy extended during the interview on February 15, 2007. During the interview, the Examiner agreed that the claims as currently drafted distinguish over the prior art of record subject to further consideration and/or search.

REJECTION UNDER 35 U.S.C. §103

Claims 1-8 and 16-22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshikawa (U.S. Pub. No. 2006/909434) in view of Takala (U.S. Pub. No. 2006/393520). This rejection is respectfully traversed.

With respect to Claim 1, Yoshikawa and Takala alone or in combination do not show, teach or suggest a control circuitry that copies display data from an external frame buffer to an internal frame buffer. The display data that is copied into the internal frame buffer is the same display data read by a display controller from the external frame buffer. Put another way, the display controller or a display receives data from the external frame buffer, which is the same data that is copied from the external frame buffer to the internal frame buffer. After the display data is copied, the same display data is located in the internal frame buffer and the external frame buffer until a new frame is available in the external frame buffer.

By loading the data in the external frame buffer into the internal frame buffer, the claimed invention allows for subsequent display refresh operations to be loaded from the internal frame buffer rather than the external frame buffer. This reduces power consumption, since in general, an internal frame buffer requires less power than an external frame buffer. The transfer also reduces bandwidth demands on the external frame buffer. In addition, by maintaining the same display data in the external frame buffer as in the internal frame buffer, the control circuitry allows for reading the same data from the external frame buffer while the internal frame buffer is loaded. This decreases display refresh time, or in other words, allows for the display to be updated quicker.

As best understood by Applicant, Yoshikawa discloses a data processing unit that includes a video controller. The video controller performs a data exchange between an internal memory and an external memory. See Abstract and col. 6, lines 20-64 of Yoshikawa. A data exchange is performed such that data that requires longer processing time or data that is more frequently accessed is mapped into the internal memory. During the data exchange, data in the internal memory is exchanged with data in the external memory. Thus, the data in the internal memory is not maintained in the external memory. The data in the internal memory is not the same as the data in the external memory. Also, the data transferred to the internal memory from the external memory is not also transferred from the external memory to a display. In Yoshikawa, data in the external memory, which is transferred to a display, is not also transferred to the internal memory.

It is admitted in the Office Action that Yoshikawa does not teach the limitation of after the display data is copied, the same display data is located in the internal frame buffer and the external frame buffer until a new frame is available in the external frame buffer. The Examiner, in the Office Action, however alleges that Takala discloses this limitation.

As further understood by Applicant, Takala discloses an integrated circuit with a local frame buffer and a display with a display frame buffer. Takala discloses a data transfer from the local frame buffer to the display frame buffer. The Examiner alleges, in the Office Action, that Takala discloses display data that is copied from the local frame buffer to the display frame buffer and that the display frame buffer is only updated after a new frame is available in the local frame buffer, and refers to col. 2, lines 1-19 of Takala. Note this is different than that claimed. The claimed limitation states that the data in the internal frame buffer is the same as the data in the external frame buffer until a new frame is available in the external frame buffer. Also, Applicant submits that in col. 2, lines 1-19, Takala states that display information is transferred from a processor to the local frame buffer, followed by updating the display frame buffer by transferring the display information from the local frame buffer to the display frame buffer. The stated section is silent with respect to maintenance of the same data in the local frame buffer and the display frame buffer. Nevertheless, Takala clearly does not state that data is transferred from the local frame buffer to the display. In Takala, data is transferred from the local frame buffer to the display frame buffer and then to the display.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior

art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. The relied upon references alone or in combination fail to teach or suggest each and every element claimed.

Also, according to established mandates of the patent laws, "[t]o establish a prima facie case of obviousness . . . there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP §2142. "The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved." *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000). The showing must be "clear and particular, and it must be supported by actual evidence." *Teleflex, Inc. v. Ficosa North American Corp.*, 299 F.3d 1313, 1334, 63 U.S.P.Q.2d 1374, 1387 (Fed. Cir. 2002) (quoting *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999)) (emphasis added). It is not sufficient to rely on "common sense and common knowledge," as there must be specific evidence to support the motivation. *In re Lee*, 277 F.3d. 1338, 1344-45, 61 USPQ.2d 1430, 1434-35 (Fed. Cir. 2002)]. It is respectfully submitted that the Patent Office has not made a legally sufficient showing of a motivation to combine based on actual, specific, evidence.

Applicant submits that it would not have been obvious to combine Yoshikawa and Takala. Yoshikawa discloses a video controller and an external memory and performs a data exchange therebetween. Takala discloses an ASIC and a display frame buffer and performs a data transfer therebetween. The arrangements of the

components of Yoshikawa are different than that of Takala. Most noticeably, Takala does not show an external memory or a memory that is external to a controller or a control circuit. Also, the video controller of Yoshikawa is coupled between the external memory and a display. On the other hand, the local frame buffer of Takala is internal to the ASIC and transfers data to a display buffer on a display.

According to MPEP §2142, "[t]o reach a proper determination under 35 U.S.C. 103, . . . impermissible hindsight must be avoided and the legal conclusion [of obviousness] must be reached on the basis of the facts gleaned from the prior art." Furthermore, according to MPEP §2143.01, "[t]he mere fact that references can be . . . modified does not render the resultant combination obvious unless the prior art also suggests the desirability of [such modification]." *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990). Since the Patent Office has offered no proper support or motivation for combining the references, it is respectfully submitted that the rejection based on obviousness is clearly and unequivocally founded upon "knowledge gleaned only from Applicant's disclosure." MPEP §2145. Consequently, it is respectfully submitted that the rejection entails hindsight and is, therefore, improper.

Therefore, Claim 1 is allowable for at least the above reasons. Claims 9 and 16 are allowable for at least similar reasons as Claim 1. Claims 2-8, 10-15 and 17-22 ultimately depend from Claims 1, 9 and 16 and are allowable for at least similar reasons.

With respect to Claim 2, 10 and 19, Yoshikawa and Takala do not show, teach or suggest the simultaneous coping of data into an internal frame buffer from an external frame buffer and reading of the data by a display from the external frame buffer. The

Examiner alleges that Yoshikawa describes display data that is copied into an internal frame buffer simultaneously with a display controller reading display data from an external frame buffer. The Examiner refers to col. 9, lines 57-67 of Yoshikawa. In col. 9, lines 57-67, Yoshikawa discloses a data exchange the transfer of data from an external memory to an internal memory and vice versa. For this reason, Claim 2 is further novel and nonobvious.

With respect to Claims 5 and 21, Yoshikawa and Takala fail to show, teach or suggest the maintaining of display data in an external frame buffer as copied to an internal frame buffer, as well as the internal frame buffer and control circuitry being disposed on a single graphics chip 10 and the external frame buffer being disposed on another chip separate from the graphics chip. The Office Action relies on Takala for disclosing maintenance of display data in an external frame buffer as copied to an internal frame buffer. The Office Action relies on Yoshikawa for disclosing an internal frame buffer and a control circuitry that are disposed on a single graphics chip and an external frame buffer that is disposed on another chip.

Note that item 10 of Yoshikawa refers to a video controller that has an internal memory 12, a processing unit 13, a D/A converter 19 and a memory control unit 15. The video controller 10 does not appear to be a chip, but rather a circuit board that has several chips attached thereto. Applicant is unable to find any reference in Yoshikawa stating that the video controller may be a chip.

As above stated, Takala fails to disclose the limitation of maintaining display data in an external frame buffer as copied to an internal frame buffer. Also, note that in Takala, a local frame buffer 12 and display server software 6 are located on an

application specific integrated circuit (ASIC) and a display frame buffer 22 is located separately in a display module. Takala does not show an external frame buffer, as claimed. The local frame buffer 12 is incorporated in and thus, is not external to or separate from the ASIC. Also, no motivation has been provided to combine and modify Yoshikawa and Takala to arrive at the claimed invention. Thus, Claims 5 and 21 are further novel and nonobvious for the above stated reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this response is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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